What is claimed is:

1. A constellation mapping apparatus comprising:

a memory, in which constellation values in one of four quadrants of each constellation are stored;

an address generation block which receives constellation point data, bits-per-symbol information, and valid symbol information indicating whether or not the bits-per-symbol information is valid, and generates address information of the memory where the constellation values corresponding to the constellation point data are stored and quadrant information indicating a quadrant where the constellation point data are placed;

a complementation logic block which complements, based on the quadrant information for the constellation point data, or does not complement the constellation values read from the memory following the address information; and

a scaling block which outputs an output of the complementation logic block or a value obtained by multiplying the output of the complementation logic block by a predetermined gain obtained based on a baud rate, which indicates a speed of transmitting the bits-per-symbol information.

2. The constellation mapping apparatus of claim 1 further comprising a latch block which performs retiming on an output of the scaling block and then outputs the result of the retiming.

3. The constellation mapping apparatus of claim 1, wherein the address generation block comprises:

a base address generator which generates a base address;

an index address generator which generates an index address; and

an adder which adds the base address and the index address.

4. The constellation mapping apparatus of claim 3, wherein the base address generator comprises:

a multiplexer which receives bits-per-symbol information and valid symbol information and selectively outputs a value of the bits-per-symbol information or 0 depending on a value of the valid symbol information; and

a shifter which shifts a predetermined value by as much as an output of the multiplexer.

5. The constellation mapping apparatus of claim 4, wherein the predetermined value is a binary number '00000001'.

6. The constellation mapping apparatus of claim 3, wherein the index address generator comprises:

a subtractor which subtracts a predetermined value from an output of the multiplexer in the base address generator;

a shifter which shifts the input data by as much as an output of the subtractor; and

a multiplexer which receives data obtained by selecting lower six bits of an output of the shifter and coupling a most significant bit among the selected lower six bits with a binary number '00000', data obtained by coupling fifth and fourth bits among the selected lower six bits with a binary number '0000', data obtained by coupling the fifth bit through a third bit among the selected lower six bits with a binary number '000', data obtained by coupling the fifth bit through a second bit among the selected lower six bits with a binary number '00', data obtained by coupling the fifth bit through a first bit among the selected lower six bits with a binary number '0', a binary number '000000', and receives an output of the multiplexer in the base address generator via a selection port.

7. The constellation mapping apparatus of claim 1, wherein in the memory, constellation values in one of the four quadrants of each of the constellations are stored in such a manner that real number components and imaginary number components of the constellation values are stored separately.

8. The constellation mapping apparatus of claim 1, wherein the complementation logic block comprises:

a complementer which receives an in-phase output and a quadrature-phase from the memory and generates negative values;

a multiplexer which receives upper two bits of an output of the shifter in the index address generator from the memory via a selection port; and

a complementation logic block which receives quadrant information indicating which quadrant the constellation points stored in the memory belong to, the upper two bits of the output of the shifter in the index address generator, and generates a control signal, which is used to determine whether to complement an output of the memory or not based on the quadrant information and information on a quadrant where the input data are placed.

9. The constellation mapping apparatus of claim 1, wherein the scaling block comprises a multiplexer which receives a seventh bit of an output of the shifter in the index address generator,

wherein the multiplexer receives an in-phase output of the complementation logic block and a value obtained by multiplying the in-phase output by a predetermined gain obtained based on a baud rate.

10. A constellation mapping method comprising:

receiving constellation point data, bits-per-symbol information, and valid symbol information indicating whether or not the bits-per-symbol information is valid;

generating address information of a memory, in which constellation values corresponding to the constellation point data are stored;

outputting an output of the memory or a result of complementing the output of the memory by generating real numbers and imaginary numbers in one of four quadrants of a constellation based on the address information of the memory; and

selectively outputting the value output in the previous step or a value obtained by multiplying the output value by a predetermined gain.

11. The constellation mapping method of claim 10 further comprising storing the selectively output value or performing retiming on the selectively output value for a following block.

12. The constellation mapping method of claim 10, wherein generating the address information of the memory, comprises:

generating a base address;

generating an index address; and

adding the base address and the index address.

13. The constellation mapping method of claim 12, wherein generating the base address, comprises:

receiving bits-per-symbol information and valid symbol information and selectively outputting a value of the bits-per-symbol information or 0 depending on a value of the valid symbol information; and

shifting a binary number '00000001' by as much as the selectively output value.

14. The constellation mapping method of claim 12, wherein generating the index address, comprises:

subtracting a predetermined value from the value generated in generating the base address;

shifting the input data by as much as the result of the subtraction; and

receiving data obtained by selecting lower six bits of the result of the shifting and coupling a most significant bit among the selected lower six bits with a binary number '00000', data obtained by coupling fifth and fourth bits among the selected lower six bits with a binary number '0000', data obtained by coupling the fifth bit through a third bit among the selected lower six bits with a binary number '000', data obtained by coupling the fifth bit through a second bit among the selected lower six bits with a binary number '00', data obtained by coupling the fifth bit through a first bit among the selected lower six bits with a binary number '0', a binary number '000000', and receiving the value output in generating the base address via a selection port.

15. A computer-readable recording medium, on which the method of claim 10 is written in computer-readable program codes which can be processed in a computer.